40M TAC Meeting
June 2009

Intro / Outline

- Crew Changes
- DRFPMI + DC Readout Locking Status
- Upgrade(https://dcc.ligo.org/cgi-bin/private/DocDB/ShowDocument?docid=231)
  - Doc on Wiki/SVN/New DCC
  - Motivation
  - Status
- Schedule

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Shift Changes

- Yoichi Aso (6/08 - 5/09) gone to U. Tokyo
- Peter Kalmus, Alberto Stochino now on graveyard shift locking w/ Rob.
- Koji Arai coming in July (part time 40m)
- New grad student, Kiwamu Izumi (from NAOJ) coming for 2-3 years
- ~1 new Caltech grad student in the fall
- Rob has never been closer to graduating…

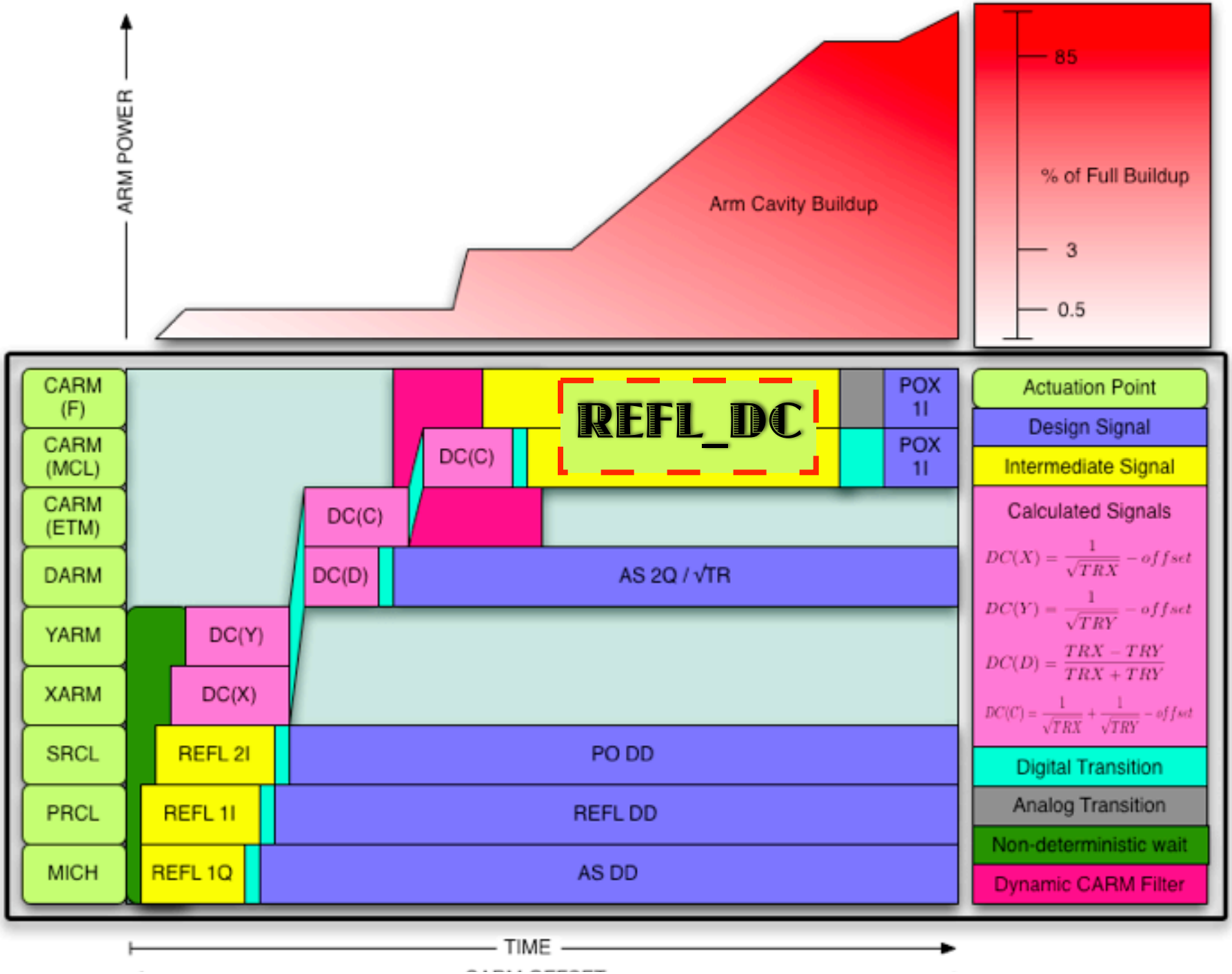
Usuals: Steve Vass, Bob Taylor, Jenne Driggers, Joe Betsweizer, Rana Adhikari, Alan Weinstein

DRSE LOCKING

- PRFPMI (eLIGO configuration) done early 2008
- DRSE w/ DC Readout in summer 2008
- Magnets broken, wires slipped in Mag 5.6 Chino quake.
- anti-spring locking re-achieved ~May 1st.
- Lock acquisition + CARM de-detune fairly robust and fast.

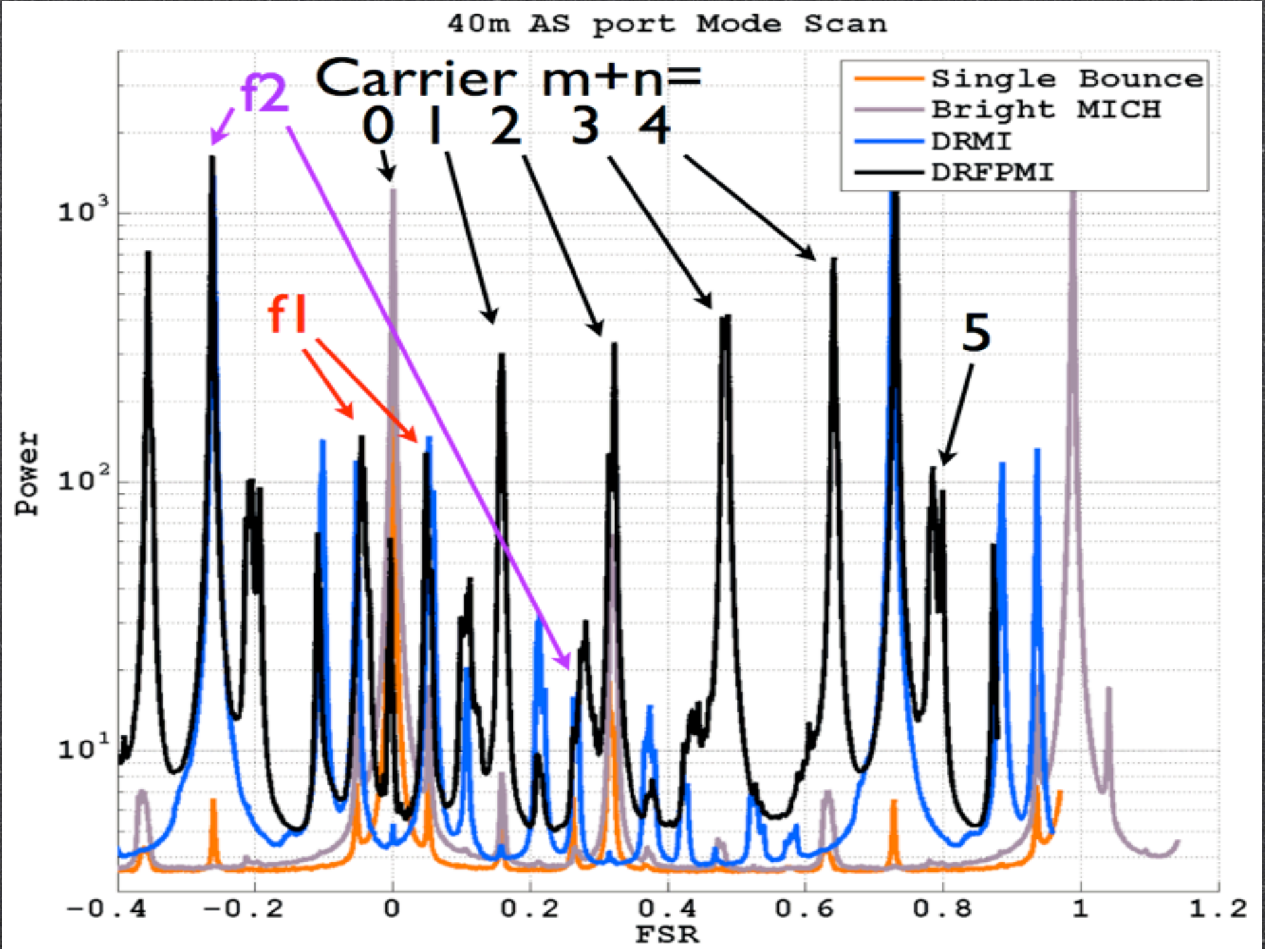
Annoying Problems

- Maglev Turbo Pump failure: temp. use noisy cryo, maglev replaced.
- ISS Oscillations: dying MOPA changes the low frequency current shunt TF.
- Flaky solder joint in MC Board AO path - SMD resistor (done by Screaming Circuits)has been in there a few years.
- Broken magnets, slipped wires, etc.
- FSS: bad AOM alignment (single pass), servo parts oscillation, Crystal RF reference dying (same symptom as LHO and LLO).
- PMC: PZT went bad slowly over many months => swapped PMC. Sent bad one to Rick Savage.
- Arm power drifts: redo coil balancing -> ~hour long locks
- MOPA Chiller plumbing broken, chiller failed: repaired chiller, reworked chiller plumbing and adding flow meters.


ARM POWER
Arm Cavity Buildup
85
% of Full Buildup
3
0.5
REFL_DC
CARM (F)
CARM (MCL)
CARM (ETM)
DARM
YARM
XARM
SRCL
PRCL
MICH
DC(C)
DC(C)
DC(D)
DC(Y)
DC(X)
REFL 2I
REFL 1I
REFL 1Q
POX 1I
POX 1I
AS 2Q / √TR
PO DD
REFL DD
AS DD
Actuation Point
Design Signal
Intermediate Signal
Calculated Signals
$DC(X) = \frac{1}{\sqrt{TRX}} - offset$
$DC(Y) = \frac{1}{\sqrt{TRY}} - offset$
$DC(D) = \frac{TRX - TRY}{TRX + TRY}$
$DC(C) = \frac{1}{\sqrt{TRX}} + \frac{1}{\sqrt{TRY}} - offset$
Digital Transition
Analog Transition
Non-deterministic wait
Dynamic CARM Filter
TIME

Interesting Problems

- 3.8 kHz peak in the CARM TF prevented detuning CARM. Traced down to be coupling of the DARM RSE peak into the PO_DC. (furious Optickle modeling ensues) Switched to REFL_DC as the intermediate CARM signal.
- DARM instabilities as CARM offset reduced. (modeling): carrier phase at AS port rotates continuously during offset reduction. Continuous rotation of DARM demod phase to compensate.
- Total Locking success rate ~30% (after initial state acquisition). CARM/MCL handoff success ~65%. REFL_DC => REFL166_I success ~ 50%.
- Exploring lock acq. w/ MC - no CARM->ETM feedback. Works OK w/ single arm. Low frequencies disturb the FSS so we did MC locking w/ no FSS.
- Locking on +spring seems tough. Long time to acquire. HOM problem?

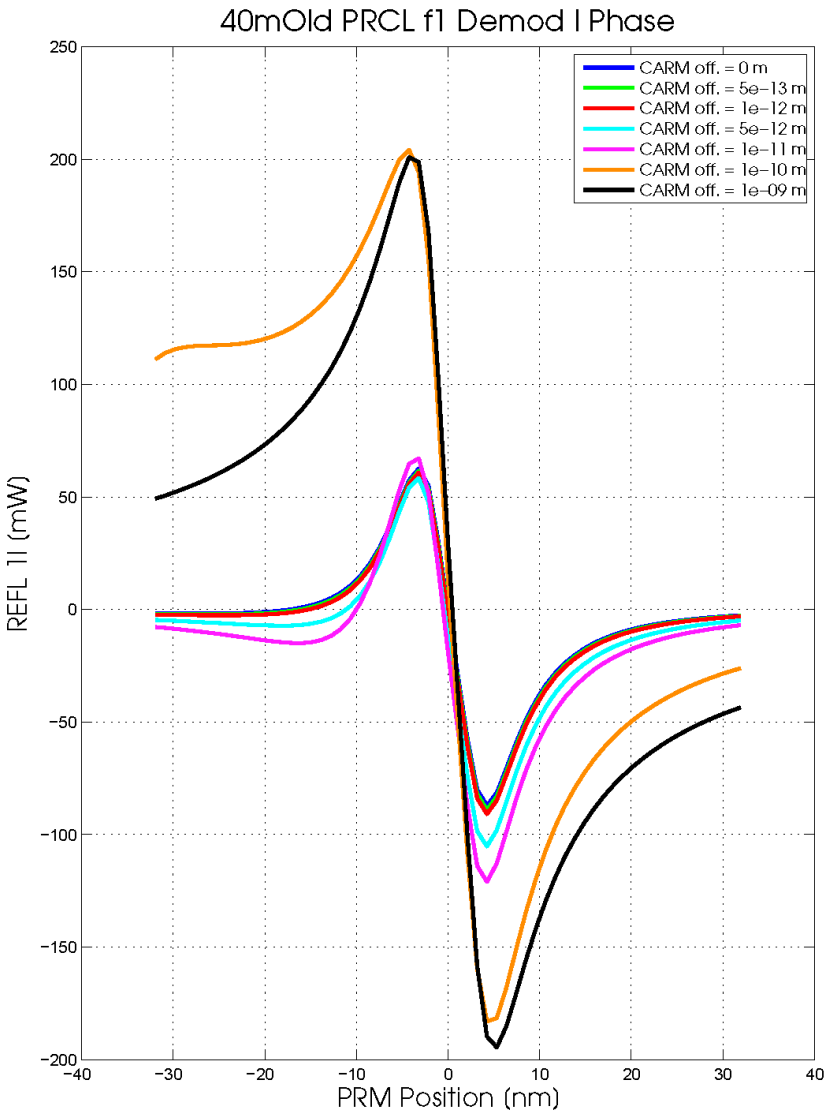

40m AS port Mode Scan
Carrier m+n=
0 1 2 3 4
5
f2
f1
Single Bounce
Bright MICH
DRMI
DRFPMI
Power
10^3
10^2
10^1
−0.4 −0.2 0 0.2 0.4 0.6 0.8 1 1.2
FSR

UPGRADE '09

- Arm Finesse : 1200 -> 450
- Mod. Freqs: 33->9 MHz, 166->45 MHz
- Recycling: Longer cavities (requires folding)
- Mach Zehnder: Gone
- Control System: Many VME->One Fast MultiCPU box
- **Adaptive NC: Adaptive FIR, Inputs from PEM**
- **Alt Locking: Green light, fiber delivery, AOM shifting**
- Misc:
  - GigE Cameras: Fast Image Processing – Fast Network
  - PEM Sensors: For FF cancellation
  - Longer Oplevs: More stable – instead of full ASC
  - Dither alignment: DC BW, Audio " WFS"

SOUTH
VERTEX
CHAMBER
(SV)
EAST
VERTEX
CHAMBER
(EV)

3f Locking



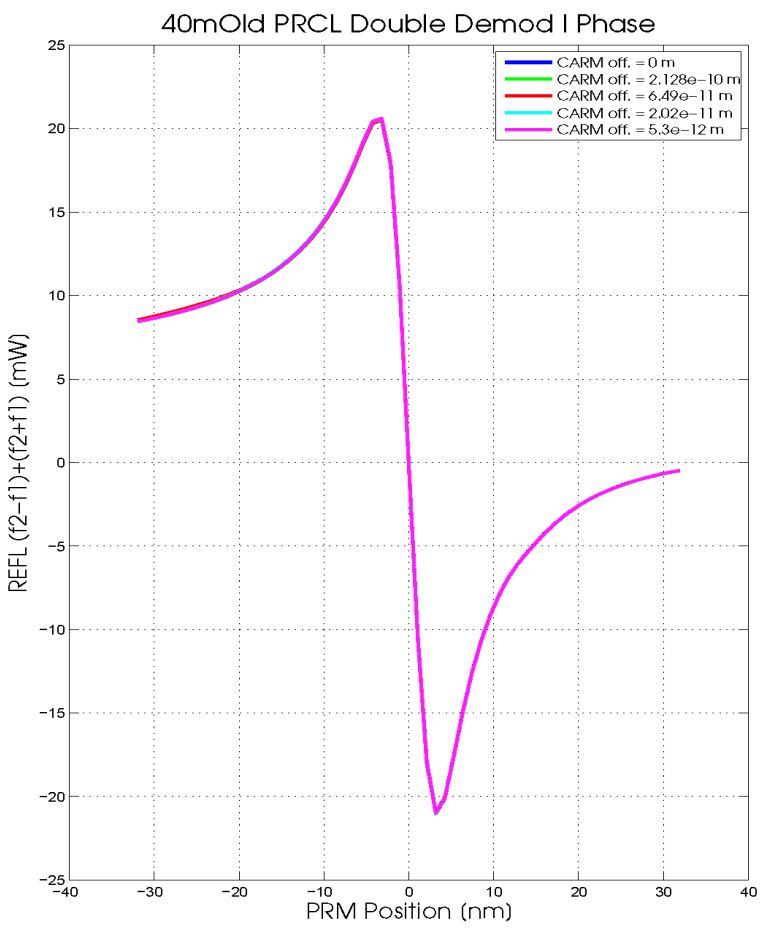
- The central DOFs cannot be maintained locked by error signals that involve the carrier while the CARM offset is reduced.
- At the 40m we use 2 modulation frequencies, 33 and 166 MHz. The beat between the two is double demodulated and provides an error signal that depends much less on the carrier.
- That double demod signal can be used only in the IFO configuration with the detuned SRM (narrow band detection).

For the broadband, configuration another control signal is needed.

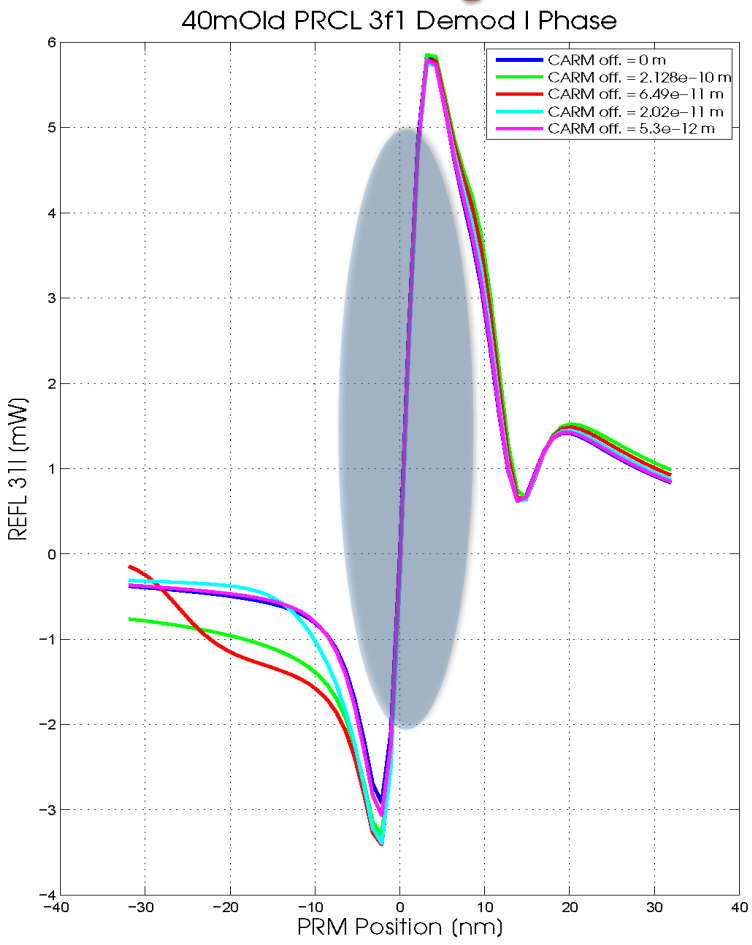
3f Locking at the 40m

- In '3f locking' the error signal is obtained by the beat between the first and the second order sidebands produced by the same modulation frequency.
- The signal can be used for lock acquisition and also in broadband configuration operation.

Double Demod Error Signal

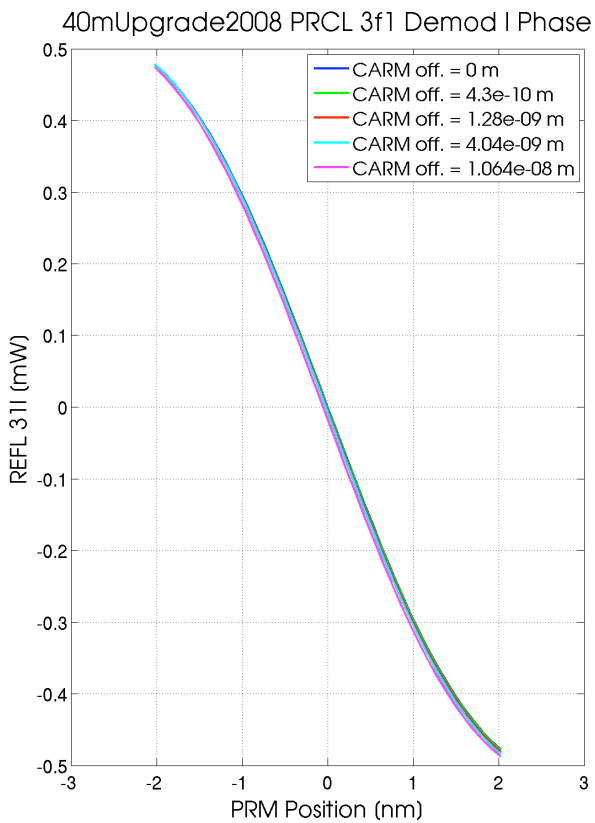


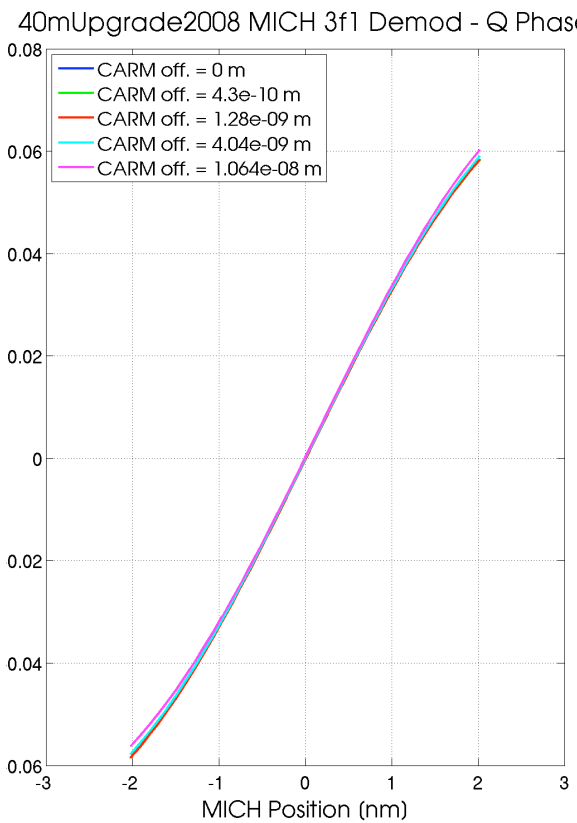
3f Error Signal

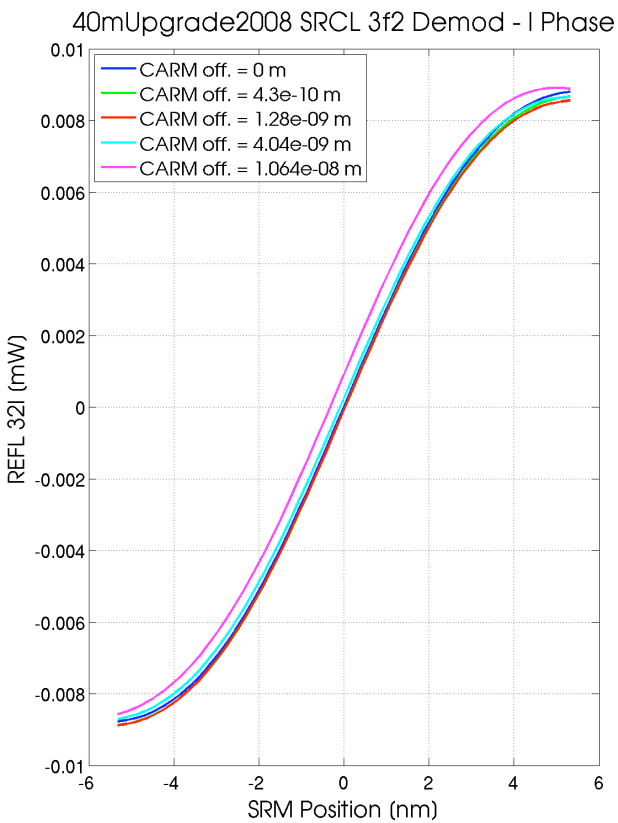


Proposed 3f Signals
f1 = 11 MHz; f2 = 55MHz

DOF	Signal	Dem freq.	Gain	Linearity Range	Shot Noise Limit
PRCL	REFL_1I	3*f1	0.2 mW/nm	4 nm	3e-16 m/sqrt(Hz)
MICH	REFL_31Q	3*f1	0.02 mW/nm	8 nm	3e-15 m/sqrt(Hz)
SRCL	REFL_32I	3*f2	0.002 mW/nm	8 nm	3e-14 m/sqrt(Hz)

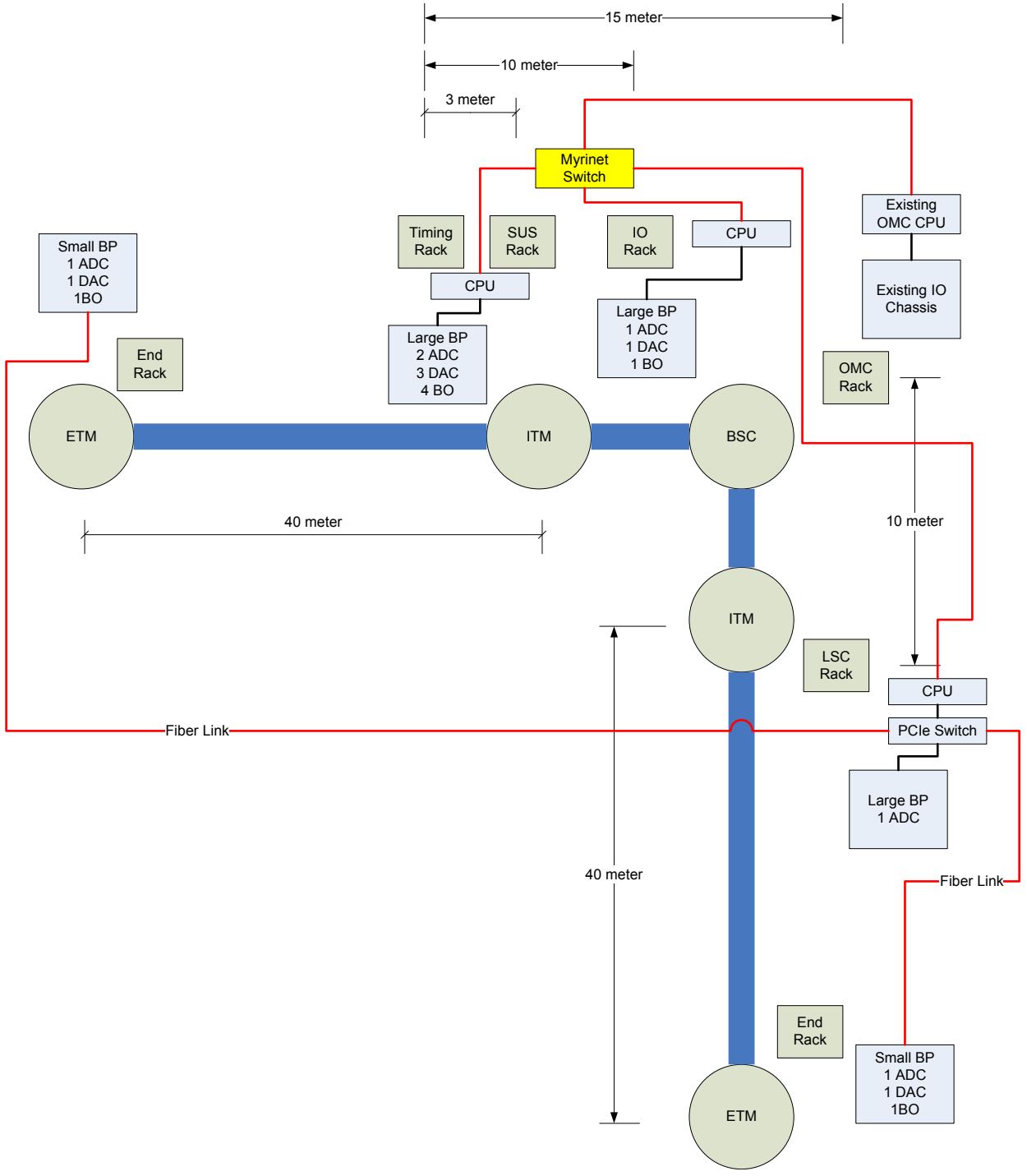






Upgrade SCHEDULE

- ATF (Ramin) has contract for ITM, PRM, SRM - specs on Wiki. Delivery due in late September.
- SOS construction by Mike Myer (LLO). They're in the mail to Pasadena.
- No MC Length change: see below.
- RC Folding mirrors (CVI Y1S? REO?) - need input.
- Mod. Freq. Choices: Decided on 11/55 MHz.
- RC Folding mirrors: *Advanced* TT from ANU.


15 meter
10 meter
3 meter
Myrinet Switch
Timing Rack
SUS Rack
IO Rack
CPU
CPU
Existing OMC CPU
Existing IO Chassis
Small BP 1 ADC 1 DAC 1BO
Large BP 2 ADC 3 DAC 4 BO
Large BP 1 ADC 1 DAC 1 BO
End Rack
OMC Rack
ETM
ITM
BSC
40 meter
10 meter
ITM
LSC Rack
CPU
Fiber Link
PCIe Switch
Large BP 1 ADC
40 meter
Fiber Link
End Rack
ETM
Small BP 1 ADC 1 DAC 1BO

CDS SCHEDULE

- ADCs, DACs, BOs, Adapter boards, IO Chassis, New CPUs, Fiber bundles, switches, in house
- Integration of many units is tricky: early AdvLIGO pathfinding
- Near term: Swap ETMX to new system
- Near term: Build New FEs offline